ABSTRACT

0029 A method for improving a polysilicon gate electrode profile to avoid preferential RIE etching in a polysilicon gate electrode etching process including carrying out a multi-step etching process wherein at least one of a lower RF source power and RF bias power are reduced to complete a polysilicon etching process and an in-situ plasma treatment with an inert gas plasma is carried out prior to neutralize an electrical charge imbalance prior to carrying out an overetch step.